PSINS: An Open Source Event Tracer and Execution Simulator for MPI Applications

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Abstract. The size of supercomputers in numbers of processors is growing exponentially. Today's largest supercomputers have upwards of a hundred thousand processors and tomorrow's may have on the order one million. The applications that run on these systems commonly coordinate their parallel activities via MPI; a trace of these MPI communication events is an important input for tools that visualize, simulate, or enable tuning of parallel applications. We introduce an efficient, accurate and flexible trace-driven performance modeling and prediction tool, PMaC's Open Source Interconnect and Network Simulator (PSINS), for MPI applications. A principal feature of PSINS is its usability for applications that scale up to large processor counts. PSINS generates compact and tractable event traces for fast and efficient simulations while producing accurate performance predictions. It also allows researchers to easily plug in different event trace formats and communication models, allowing it to interface gracefully with other tools. This provides a flexible framework for collaboratively exploring the implications of constantly growing supercomputers on application scaling, in the context of network architectures and topologies of state-of-the-art and future planned large-scale systems.

Keywords: High Performance Computing, Message Passing Applications, Performance Prediction, Trace-Driven Simulation, and Supercomputers.

1 Introduction

Performance models are calculable expressions that describe the interaction of an application with the computer hardware providing valuable information for tuning of both applications and systems [1]. An ongoing trend in High Performance Computing (HPC) is the increase in the total system core count; this in turn has enabled scaling to tens and even hundreds of thousands of cores in recent years enabled by performance models that are used to guide application tuning [2-4]. Application performance is a complex function of many factors such as algorithms, implementation, compilers, underlying processor architecture and communication (interconnect) technology and topology. However as applications scale to larger processor counts, the interconnect becomes a more prevalent factor in their performance requiring improved tools to measure and model it.

We present an efficient, accurate and flexible trace-driven performance modeling tool, PMaC's Open Source Interconnect and Network Simulator (PSINS), for MPI applications. PSINS includes two major components, one for collecting event traces during an application's run (*PSINS Tracer*), and the other for the replay and simulation of these event traces (*PSINS Simulator*) for the modeling of current and future HPC systems. The key design goals for PSINS are 1) scalability 2) speed 3) extensibility. To meet the first goal PSINS Tracer runs with very low overhead to generate compact traces that do not use more bits than are needed for a complete record of events; to meet the second goal PSINS Simulator enables replay of events faster than real-time (a replay does not normally take as long as the original application run) while still producing accurate performance predictions. To meet the third goal, both PSINS components, Tracer and Simulator, are provided freely as open-source, and have, in addition to its built-in trace formats, format conversion modules, and communication models, a graceful API designed such that anyone can easily extend these tools via plug-in virtual functions. PSINS interacts gracefully with other popular tracers and modeling and visualization tools such as that presented by Ratn et al. [5], MPIDtrace [6], Dimemas [7], TAU [8] and VAMPIR [9]. Figure 1 below shows the high-level design of PSINS as well as the flow of information that occurs for performance prediction.

1.1 Tracer for Collecting Event Traces

PSINS provides a tracer library based on MPI's profiling interface (PMPI) [10]. PMPI provides the means to replace MPI routines at link time allowing tool developers to include additional instrumentation code around the actual MPI calls. In addition, the PMPI interface enables gathering detailed information about the arguments to each MPI call by sharing the same signature as the actual invocation.

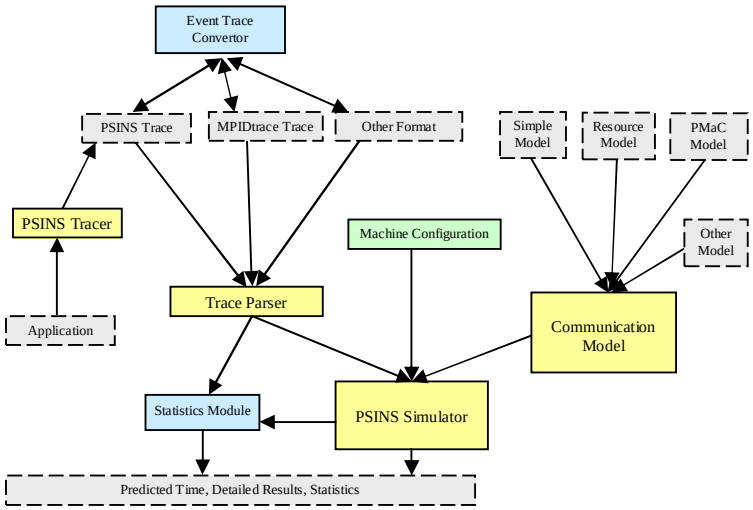


Figure 1. The high-level design of PSINS as well as the flow of information.

The tracer library provides wrappers that serve as replacements for the MPI routines in the code (i.e. communication or synchronization events). For each MPI routine replacement, it uses additional code to gather detailed information about the called MPI function and its arguments. The tracer also gathers the time in between individual communication events or the computation time, labeled as *CPUBurst*. To gather CPUBurst events, the library uses timers at the end and the beginning of each MPI routine replacement so that when an MPI function is called, the time spent since the end of the last MPI call to the current call is recorded in the trace.

Since HPC applications typically run for long duration and tend to execute millions of MPI function calls, recording each event to a trace file as it occurs is not practical due to the many small, latency-bound file I/O accesses that would induce. Like other efficient tracing tools [11,28-29], PSINS Tracer uses per-task local memory buffers to temporarily store event information and only dumps the events when the buffer for the task is full. Moreover, to eliminate the need for any additional communication due to tracing, PSINS Tracer initially generates a separate event trace file for each MPI task in the application.

In a post-trace phase, to combine these separate trace files in to a single compact trace file, PSINS includes a trace consolidation utility, *mpi2psins*. This is done serially after the execution of the traced application. This mpi2psins utility uses an encoding mechanism similar to general UTF encodings [12] in order to reduce the size of the final trace. It uses the most significant bit in each byte to determine the number of bytes that will be used to represent a number and the other seven bits to store the actual value. Using this technique it is possible to represent 2^{7n} possible values with n bytes. An event trace is made up mostly of small integers that represent processor IDs, larger integers that represent message sizes, and real numbers that represent times. On average our encoding saves 60% of the size that would be required if these values were kept as normal 4 byte or 8 byte values. The trace thus serves as a minimal complete representation of events to which further compression techniques such as those that detect and encode regular expressions can be applied [26]. More importantly, as described in the results section, when carrying out strong scaling studies, the size of communication traces encoded by this method grows linearly as function of processor count *even though the global communications may grow exponentially* [27]. This is because the time becomes shorter (at least for scalable codes) and the message sizes tend to decrease, with increasing processor count, and thus the UTF encodings become smaller with increasing processor count even though the total number of communications may go up.

Besides tracing functionality, PSINS tracer provides two additional libraries for performance measurement and analysis that can be included in the event trace run or collected independent from the trace. The first, called *PSINS Light*, is a library to measure overall execution time of the application and gather some event counts from the performance monitoring hardware (using PAPI [15]) in the underlying processors such as FLOP rate and cache miss counts. The second, called *PSINS Count*, is a library to measure the execution times and frequencies of each MPI function in the application in addition to those values collected by PSINS Light. PSINS Count is similar to IPM [14] and provides only a subset of information IPM provides. PSINS Tracer library is already ported for several HPC systems and is available at http://www.sdsc.edu/pmac/projects/psins.html.

1.2 Adding a New Input Trace Parser

In PSINS, the trace parser module is included as a separate module to allow the simulator to use different input trace formats easily. This allows users to easily add another trace format such as TAU in addition to the already included parsers for PSINS and the MPIDtrace trace formats. A trace consists of a sequence of events that occur for each task and to use another trace format, the new parser needs only to convert events to the PSINS internal representation of trace events.

In PSINS a new trace parser is added via use of virtual C++ functions. PSINS provides a base class, *Parser*, with a few virtual methods (see technical report [13] for the list of these virtual methods and more detail). These virtual methods provide minimal functionality to access and consume the input trace.

Even though adding new parsers to PSINS requires some coding knowledge, PSINS hides most of the complexity of this process by providing most of the common infrastructure that is used by all parsers, requiring only the implementation of a few virtual methods. For example the parser for PSINS built-in trace format requires only 384 lines and the parser for MPIDtrace format requires 647 lines of C++ code.

1.3 Simulator for Performance Prediction

PSINS Simulator takes the communication event trace for an application and a set of modeling parameters for the target system and then replays the event trace for the target system, essentially simulating the execution of the parallel application on the target system. To simulate an MPI application on a target system, PSINS models both computation and communication times for each task in the application.

To simulate the execution of a target system, the simulator needs details about the configuration and construction of the system. These modeling parameters consist of configurable components of a parallel HPC system.

To begin with, PSINS assumes that the target architecture is a parallel computer composed of multiple computation nodes connected via configurable number of global busses (as shown in Figure 2). Each computation node contains a configurable number of processing units (processors or cores) and incoming and outgoing links to the global busses. It provides the flexibility for each compute node to have different numbers of incoming and outgoing links to the global busses and different number of processing units in the node. In addition, the processing units within a compute node can be specified to have different speeds. By relaxing the restrictions on the target system architecture, PSINS provides the capability to simulate varying types of systems ranging from computational grids to shared memory multiprocessor systems.

All of these configurable modeling parameters are given to simulator in a small ASCII configuration file. The configuration file contains parameters for the system as a whole, for each compute node and for the MPI task-to-processor mapping. For the system, required parameters include the number of compute nodes, the best achievable bandwidth and latency for each bus for two nodes to communicate, and the number of busses. For each compute node, required parameters include the number of processing units, the number of incoming and outgoing links from/to busses, the best achievable local bandwidth and latency within the node, a mapping of MPI tasks to

processors, and CPU ratios which describe relative speeds (ratios) for the computational work of the target with respect to the base system. This CPU ratio is used by PSINS to model the computation time. This is done by simply projecting the time spent for each CPUBurst event to the target system using the multiplicative factor of how much faster or slower the processing unit in the target system is relative to the base system. This approach is shown to be effective in previous research [1,6].

By separating the parameters for the target system from the communication model used for the simulation (as shown in Figure 1), PSINS allows even more flexibility toward investigating the impact of different communication models. The PSINS built-in communication models are described in detail in Section 2.1.

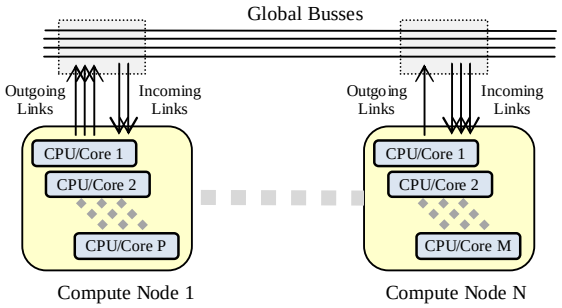


Figure 2. Target architecture for simulation

PSINS Simulator consumes events from the input trace in the order of their execution within the simulator rather than consuming them on a per-task basis. The simulator uses an event queue based on priority queues to replay the input trace.

When an event is read, it is tagged with the earliest time it will be ready for execution as its priority. This time is the value of the per-task timer at the time of insertion for the task that event belongs to. If an event is not ready for execution such as a blocking receive, or global communication, it is re-inserted into the event queue for later processing with its priority reduced. An event is deleted from queue when its execution is over. When an event is executed, it is marked with its execution time as well as its wait time. The wait time is a record of time the event had to wait for its execution as in imbalanced parallel applications with blocking communications or barriers. After its execution, the execution timer for its task is incremented accordingly and global timer is updated for synchronous simulation.

The execution of an event during simulation depends on the type of the event and the state of the system at each event execution. The state of a system at any given time is a combination of the best achievable bandwidths and latencies, the bus load, contention, traffic in the network and the underlying network topology. If it is a CPU burst event, it is completed by calculation of its time on the target system using the CPU ratio described above. For blocking communication events, it is kept in the queue until its mate is posted. If the event is a global communication, it is kept in the queue until all participating tasks post the same event. When all participating tasks post the event for the communication, communication model is asked to calculate the bandwidth and latency at the time of its execution and the event is executed. Each event type can have a different model based on network or system configuration.

PSINS Simulator includes a statistics module to collect detailed information about the simulation of an event trace on the target system, similar to IPM. The statistics module collects information about the event execution frequencies, computation and communication times for each task as well as the execution time for each event type on the target system. It also collects the waiting time for each event type to provide information on load balancing during the execution. Moreover, it generates histograms on message sizes and on the ranges of bandwidths calculated by the communication model for the communication events.

Such information provides valuable feedback to users and developers to help them understand the interaction of applications with the target system, and can be valuable to guiding optimization efforts for the application. More importantly, this information is useful for verifying simulation accuracy by comparing it to the same information measured during an actual run on the target system using performance monitoring tools such as IPM, TAU or PSINS Count.

2 Communication Models

PSINS isolates the modeling parameters and communication models from the simulator to enable users to easily investigate new communication models. From the perspective of the PSINS Simulator, the communication model is a black box.

The communication model takes an event, the parameters from the configuration file, and the current state of the simulated system to calculate the sustained latency and bandwidth for the messages that are associated with that event. The model is responsible for determining when an event will be executed, which might be at some point in the future due to the unavailability of resources or some other measure of contention. The model also determines which resources it will require and for how long the resources are required, which in turn can change the state of the simulated system based on the needs of the event. The communication model then calculates the time to complete the event including the time to transmit a message as well as the time that the message must wait for resources (wait time).

Each event can have its own model. These models can be simple (i.e. based on bandwidth and latency) or more complex functions of the systems state, the number of processors involved in the event, and the scalability of the event on the network.

2.1 Built-in Models

PSINS includes several built-in communication models that can be used to investigate a target system. These models are the *simple* model, the *resource contention* models, and the *PMaC* model. Our experience [16] indicates that these models can accurately be used to model application performance for a majority of today's HPC systems.

The simple model uses the best sustainable bandwidth and latency from the configuration file and assumes the resources available to the system are infinite. That is, when a message is ready to be sent, it assumes that resources along the path of the message are available and calculates the time to send the message as a simple addition of latency to the time spent to transfer the message body. For collective

communications, this model uses a simple description for each communication event that indicates whether that event scales in linear, logarithmic or constant time with respect to the number of participating tasks. The simple model is designed to model the lower bound for the communication time for an application.

As an extension to the simple model, PSINS provides three resource contention models based on the number of global busses, incoming, and outgoing links from compute nodes. These are called *bus-only*, *incoming-link-only*, and *outgoing-link-only* models. Unlike the simple model, these models assume that the number of a certain type of resource that is available for communication is limited and use a scheduling algorithm to schedule each message based on resource availability. These models are designed to investigate the impact of resource contention on the performance of an application. For instance, by predicting the performance of an application for an increasing number of busses, users can get a feel for how sensitive the application's performance is to number of busses available, which in turn can identify whether the application posts multiple messages at around the same time.

In addition to simplistic models, PSINS also includes a more complex communication model, called the PMaC model. This model is more complex than the previous models in order to increase the accuracy of the simulations. For point-to-point communications, this model takes the number of outstanding messages at the time of a message delivery and, based on the current load on the busses and input and output links, scales the maximum bandwidth accordingly.

For collective communications, alternative to using simple description of each MPI collective communication routine, the PMaC model also provides the means to use a more complex and realistic bandwidth calculations based on message sizes. This is done via measuring the bandwidth for each collective communication routine for an increasing size of messages using the synthetic benchmark, *PSINSBench*, included in PSINS package (see technical report [13] for more details). Then using a curve-fitting algorithm the measured bandwidths are fit to a continuous function and the function is later used by the model to calculate the bandwidth for a given message size. The PSINS Simulator is available at http://www.sdsc.edu/pmac/projects/psins.html.

2.2 Adding a New Model

In addition to the built-in models, PSINS allows users to easily plug-in new communication models. Like trace parsers, new communication models are added via use of virtual C++ functions. PSINS provides a base class, *Model*, with some virtual methods (see [13] for the list of virtual functions). These virtual methods provide the functionality to schedule events on resources as well as to calculate the time it takes to execute an event. Then, to create a new communication model, the user needs to define a class that extends the Model class and implement its virtual functions.

Much of the burden of the model developer then resides in the areas that are almost completely model-specific, which leaves only a few virtual functions for the developer to implement. Among the built-in models in PSINS, the simplest model requires 228 lines of C++ code. A collection of resource contention models requires 158 lines of C++ code and the most complex model requires 433 lines of C++ code.

3 Experimental Results

To demonstrate the usability, efficiency and accuracy of PSINS Tracer and Simulator, we have conducted several experiments where we used PSINS Tracer to collect MPI event traces for three scientific applications: AVUS [17], HYCOM [18] and ICEPIC [19] from the TI-09 Benchmark Suite [20]. The traces were then simulated for a set of target HPC systems and the results of these simulations were compared to the actual measurements gathered on the target systems.

All the traces were collected on a base system, NAVO's IBM Cluster 1600 (3072 cores connected with IBM's High Performance Switch), called *Babbage*. We ran the scientific applications with two input data sets, namely *standard* and *large*, and processor counts ranging from 59 to 1280. The actual runtimes for the applications range from 0.5 to 2.5 hours where each application runs for around half an hour at the highest processor count and was scaled to that count using the same input data set (i.e. strong scaling). For replay and simulation of the collected traces, we ran the simulator on a Linux box with two dual-core processors. In addition to simulating the base system Babbage, we also simulated the MHPCC's Dell Cluster, called *Jaws* (5120 cores connected with Infiniband) and ERDC's Cray XT3 system, called *Sapphire* (8320 cores connected with Cray SeaStar engine). We present results of these experiments in terms of event trace sizes, simulation times, and prediction accuracy.

3.1 PSINS Trace Sizes and Simulation Times

The sizes of traces collected for each application and processor count is given in Figure 3. The figure illustrates that the size of PSINS event traces grows linearly as the processor count grows. The sizes range from 4GB to 32GB and are more than 4 times smaller than the event trace sizes generated by a similar state-of-the-art MPI event tracer [6].

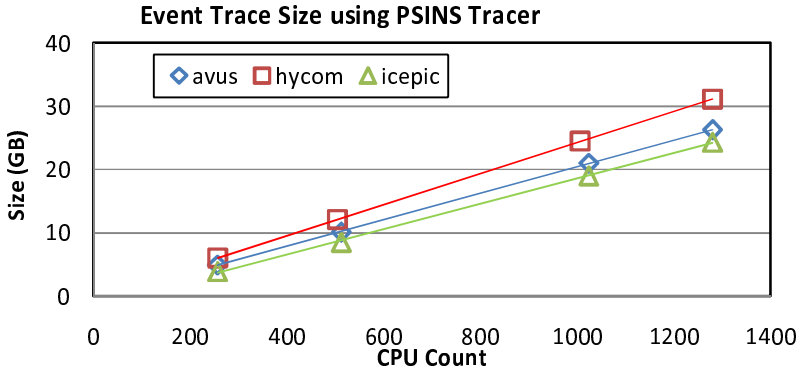


Figure 3. PSINS event trace size vs. CPU count for 3 applications.

The results suggest that one could practically store uncompressed traces for 10 thousand processors in about 300GB and would need ~3TB for 100 thousand

processor jobs. Some compression techniques such as those used in [26] would be useful at large scale though we note some research groups already devotes multiple TBs to keeping memory traces of strategic applications [25] so that same amount of storage devoted to communications traces is not out of the question.

These collected event traces were then fed through the PSINS Simulator, the simulation times are presented in Figure 4. The figure shows that PSINS Simulator is able to replay these collected traces for a target system in under 1 hour for all applications. On average the replay takes 7x less time than running the program initially did, however the replay time also grows linearly with processor count suggesting that in the future the replay procedure should itself be parallelized using natural synchronization points at global communications (planned future work) for tractable replay at tens of thousands cores. These simulation times are however already an order-of-magnitude faster than a similar network simulator [6].

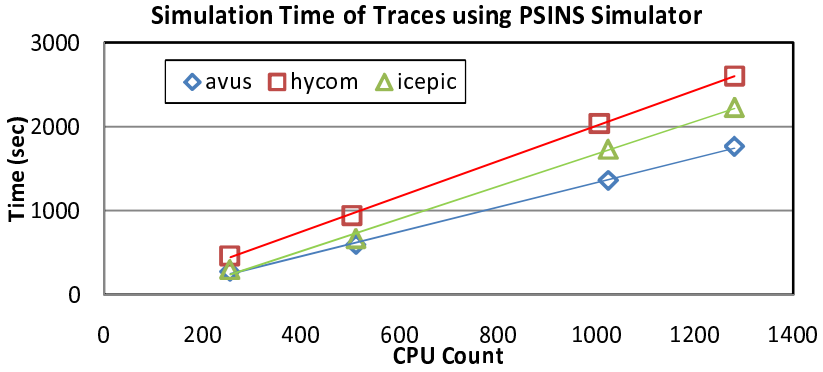


Figure 4. PSINS Simulator simulation time vs. CPU count for 3 applications.

Overall, Figure 3 and Figure 4 show that for each application, there is a linear correlation between the input trace size and the time it takes to replay the trace for a target system in PSINS. They also demonstrate that PSINS Tracer collects MPI event traces of manageable and tractable sizes and PSINS Simulator replays these traces in a tractable time for a target system. This indicates that as applications scale to even larger processors counts, PSINS is likely to continue to be usable and effective.

In addition to trace size and simulation time, it is also important to quantify the overhead introduced by the PSINS Tracer itself during trace collection. During our experiments, we observed that the overhead of PSINS Tracer ranges from 0.2% to 14.8% compared to the original execution times of the applications. The average overhead for all applications and processor counts is 5.9% meaning it can be efficiently used for large processor counts even in production runs.

3.2 Simulation Accuracy

Even though the usability of PSINS in terms of event trace sizes and simulation efficiency and tracing overhead is important, what matters most is the accuracy of the predictions produced by the models. To investigate accuracy at a finer granularity, we

simulated an event trace collected using PSINS Tracer for HYCOM with 124 processors for the base system and compared the communication times simulated to the measured times for each task. We further broke down the communication time per MPI event and compared those simulated times with the measured times. We used the built-in simple communication model in PSINS for the simulation of this application.

Figure 5 presents the communication times measured and predicted for each task. The red vertical bars are used to represent the measured times whereas the green horizontal line is used to represent the simulated times. Figure 5 shows that PSINS Simulator is quite accurate in predicting the communication time for each task. The average absolute error in predicting the communication times for all tasks is 17% whereas the error in predicting the total communication time is 14%. More importantly, Figure 5 shows that despite the imbalance in communication times among tasks, the results of PSINS simulation closely match the observed behavior.

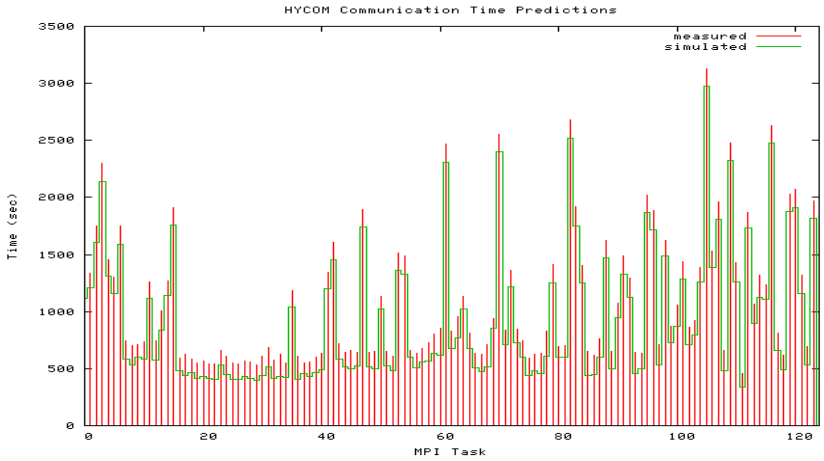


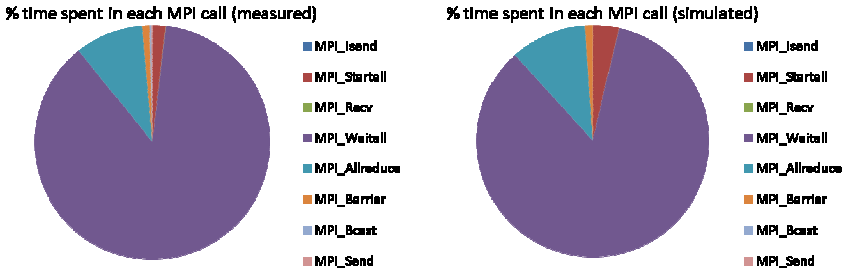
Figure 5. Measured and simulated communication times for all tasks.

Figure 5 also shows that PSINS Simulator tended to slightly under-predict the communication times for majority of the tasks compared to the actual communication times measured. This is due to the fact that we used the built-in simple model that assumes no contention just to show its effectiveness. If desired, for lower error, users can use one of the other more sophisticated built-in models.

In addition to comparing communication times for each task, we further broke down the communication time into the time spent in each MPI routine. Figure 6 (a) presents the measured values for the percentages of time spent in each MPI routine over the total communication time whereas Figure 6 (b) presents the percentages for the PSINS simulation. Figure 6 shows that the percentage of time spent in MPI routines from the simulation closely matches the percentages from the actual run, indicating the accuracy of PSINS at a finer granularity.

Table 1 presents the comparison between the total communication times measured during an actual run and times simulated by PSINS Simulator for two HPC systems. We used the more detailed PMaC model for the simulations listed in this table; it shows the ability to predict the communication times of applications within 15% error

for all cases except AVUS running with 64 processors on Sapphire. The absolute average error among all cases is only 9.0%. In AVUS with 64 processors on Sapphire, the communication time is only 7% of overall execution time. Overall, Table 1 demonstrates that PSINS is effective in modeling and predicting the performance of applications for target HPC systems.



(a) **(b)**

Figure 6. Communication time spent in MPI calls for HYCOM.

	CPU Count	Jaws			Sapphire		
		Simul.	Predict.	% Error	Simul.	Predict.	% Error
HYCOM	124	121,476	128,285	-5%	161,055	167,620	-4%
HYCOM	504	449,646	519,335	-13%	573,365	621,793	-8%
AVUS	64	27,764	26,194	6%	30,680	22,561	36%
AVUS	1280	1,333,414	1,193,967	12%			
ICEPIC	64	72,144	71,073	2%	89,950	88,708	1%
ICEPIC	1280	1,178,914	1,142,970	3%			

Table 1. Total time (in seconds) spent in communication events.

4 Related Work

Early work on performance prediction of HPC applications was done in the Proteus simulator [21], an execution-driven simulator which met many of the design goals that have been laid out for PSINS at the time. Proteus was designed modularly so that it could be customized for the target system and tradeoffs could be made between accuracy and efficiency by using a different implementation of a certain simulation component. Unfortunately Proteus introduces a slowdown of 2-35x for each process in the target application, which renders it cumbersome for the purpose of simulating long-running large-scale applications at thousand of processors.

Later work, such as Parallel Proteus [21], LAPSE [22], MPI-SIM [23] and the Wisconsin Wind Tunnel [24] improved the efficiency of the simulation required to make predictions by executing simulations in parallel. Typically these tools are execution-driven and perform parallel discrete event simulation and tend to be full machine simulators that address many aspects of a target architecture other than the

network. This causes them to be slower and more complex and less modular than PSINS for the purpose of MPI scaling investigations.

The Dimemas project [7] uses the concept of largely divorcing network prediction from the prediction of serial computation portions of the code. Like PSINS, the user supplies Dimemas with a speedup ratio for a target system. Dimemas uses this speedup ratio along with the MPI event trace (in their case called an MPIDTrace) to perform a discrete event simulation of the application on a target system. Unlike PSINS, Dimemas is not open source, hence though useful it is not quite satisfactory as a medium for community development in this arena. Dimemas currently stores their MPI event traces as an ASCII text file resulting in large event traces files.

5 Conclusions

Performance models can provide valuable information in tuning of both applications and systems, enable application-driven architecture design and extrapolate the performance of applications on future systems. In the constantly changing and growing field of HPC, it is important to have a modeling tool that is flexible enough to adapt to architectural changes and is scalable enough to grow with the constantly increasing system sizes. PSINS has this flexibility and scalability along with specific features that make it practical to use for model generation. PSINS tracer allows event traces to be captured with low overhead and recorded at manageable sizes even for large processor counts of MPI applications. PSINS simulator is capable of simulating different HPC networks with a high degree of accuracy in a reasonable amount of time. This makes PSINS is a multifunctional tool of which flexibility, scalability, and accuracy allow its utilization in collaborative studies involving modeling large scale HPC applications.

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