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**RESEARCH INTERESTS**: Performance modeling and evaluation, emerging technologies in processor architectures, IO, and memory, high-performance computing, benchmarking and simulation, energy-efficient computing.

**EDUCATION:**
**Ph.D. in Computer Science, Dec 2009, University of Texas at El Paso (UTEP)**
Ph.D. Dissertation: *Improving Throughout of Simultaneous Multithreaded (SMT) Processors using Shareable Resource Signatures and Hardware Thread Priorities*
**M.S in Computer Science, Dec 2000, University of Texas at El Paso (UTEP)**
**B.E. in Computer Engineering, University of Mumbai**

**RESEARCH EXPERIENCE**
**Jan 2010 – Present, Senior Computational Scientist, San Diego Supercomputer Center (SDSC) at UC San Diego**
Summary: Developing novel research methods for parallel program modeling and analysis, developing and analyzing software and hardware techniques memory, chips and storage to meet energy, performance, thermal, and resiliency challenges in high performance computing. Some projects are listed below:
- Developing time prediction methods on voltage scaling processors for the development of energy efficient scheduling.
- Developed SHMEM One-sided communication tracing benchmarking and simulation library.
- Developed models to predict runtime of cpu-based applications on accelerators such as GPUs and FPGAs.
- Developed capabilities to model DISK I/O time of applications on SSDs and disk drives

**Jan 2003 – Dec 2009, Research Associate with Dr. Patricia J. Teller, UTEP, Department of Computer Science**
Ph.D. dissertation: Achievable throughput in SMT processors is impeded by contention for shared resources and prompting many to disable SMT. In my dissertation I solved the problem by developing a novel method to use available hardware thread prioritization mechanisms in real systems to influence and reduce contention and increase achievable throughput. I developed a new application characterization method called Shared Resource Usage (SRS) signatures. I developed new prediction methods that use SRS signatures to predict best thread priority assignments for an application pair.

I was supported as a RA during my Ph.D. studies where I had various projects and roles which are summarized below:
- Performance evaluation research to evaluate and analyze bottlenecks in Virtualization technology for ERP architectures.
- Development of dynamic adaptive algorithms for PDE solvers to meet runtime guarantees
- Research support for tools, user training, support for cluster systems, SMP machines, and porting HPC applications

**INDUSTRY EXPERIENCE**
**Aug 2004 – Dec 2004, Engineering Intern, Intel Corporation, Hillsboro, OR**
- Developed a suite of testing patterns that validated the clock circuit of a Pentium IV processor.

**Jul 2002 – Aug 2002, Network Administrator, TCEQ Agency**
- Support for laptop, desktop and networking hardware

**Mar 2001 – Nov 2001, Software Engineer, Motorola, Inc, Fort Worth TX**
- Developed a suite of APIs for Man-to-Machine interface (MMI) software for testing cellular base stations.

**TEACHING EXPERIENCE**
**Spring 2007, Fall 2002, Spring 2002, Teaching Assistant, UTEP, Department of Computer Science**
- Courses: Computer Architecture, DBMS, Computer Networks, Distributed computing

**Aug 1999 – Dec 2000, Teaching Assistant, UTEP, Department of Computer Science**
- Courses: Algorithms, Intro to C, Intro to Pascal

**PUBLICATIONS:**
- **M. R. Meswani**, L. Carrington, et al., "Modeling and Predicting Performance of HPC Applications on Hardware Accelerators," To Appear *in the Int'l Journal of High Performance Computing (IJHPCA)*.
- **M. R. Meswani**, L. Carrington, et al., "Tools for Benchmarking, Tracing, and Simulating SHMEM Applications," To Appear at the *Cray User Group (CUG) Conference*, 2012.
- **M. R. Meswani**, L. Carrington, et al., "Modeling and Predicting Performance of HPC Applications on Hardware Accelerators," To Appear at the *Workshop on Accelerators and Hybrid Exascale Systems (AsHES), held in conjunction with IPDPS*, 2012.

- **M. R. Meswani**, L. Carrington, et al., "Modeling and Predicting Performance on Hardware Accelerators," To appear as a *Poster at the International Symposium on Workload Characterization (IISWC)*, 2011.
- M. Laurenzano, **M. R. Meswani**, et al., "Reducing Energy Usage with Memory and Computation-Aware Dynamic Frequency Scaling," To appear in *Proceedings of Euro-Par 2011,* Bordeaux, France, Aug 2011.
- **M. R. Meswani**, J. He, et al., "Modeling and Predicting disk I/O on flash systems," in *Proceedings of Workshop on the Application of Communication Theory to Emerging Memory Technologies*. Miami, Dec 2010.
- C. Olschanowsky, **M. R. Meswani**, et al., "PIR: PMaC's Idiom Recognizer," in *Proceedings of Parallel Software Tools and Tool Infrastructures (PSTI 2010) held in conjunction with ICPP 2010,* San Diego, CA, Sep 2010.
- **M. R. Meswani**, M. Laurenzano, et al., "Modeling and predicting disk I/O time of HPC applications," in *Proceedings of 2010 User Group Conference (UGC 2010)*, Schaumburg, Il, Jun 2010.
- **M. R. Meswani**, *Improving Throughout of Simultaneous Multithreaded (SMT) Processors using Shareable Resource Signatures and Hardware Thread Priorities,* Ph.D., dissertation, University of Texas at El Paso, College of Engineering – Computer Science, Dec 2009.
- **M. R. Meswani**, P. J. Teller, and S. Arunagiri "Improved Throughput of Simultaneous Multithreaded (SMT) Processors using SMT Thread Signatures and Hardware Thread Priorities," Poster at the *10th LCI International Conference on High-Performance Clustered Computing (LCI'09)*, Bolder, CO, March 2009.
- **M. R. Meswani**, P. J. Teller, and S. Arunagiri, "Measuring and Validating Metrics used to Estimate Microarchitecture Resource Utilization: A Case Study of the IBM POWER5 Processor," Poster at *the 2008 ITEA Live-Virtual-Constructive Conference*, El Paso, TX, Jan 2009.
- P. C. Trillo, **M. R. Meswani**, et al., "A Study of the Influence of the POWER5 Dynamic Resource Balancing Hardware on Optimal Hardware Thread Priorities," in *Proceedings of the 2008 ITEA Live-Virtual-Constructive Conference*, El Paso, TX, Jan 2009. **(Best Undergraduate Paper Award to P. C. Trillo)**
- **M. R. Meswani**, "Improving Throughput of SMT Processors using Application Signatures and Thread Priorities," *Presented at* the Doctoral Showcase at *SC08, the 21$^{st}$ International Conference for High Performance Computing, Networking, Storage and Analysis*, Austin, TX, Nov 2008.
- **M. R. Meswani**, and P. J. Teller, "Evaluating the Performance Impact of Hardware Thread Priorities in Simultaneous Multithreaded Processors using SPEC CPU2000," in *Proceedings of the 2$^{nd}$ International Workshop on Operating System Interference in High Performance Applications*, in conjunction with the PACT06 Conference, Seattle, WA, Sept 2006.
- D. Villa, **M. R. Meswani**, et al., "Profiling Memory Subsystem Performance in an Advanced POWER Virtualization Environment," *in Proceedings of the 1$^{st}$ International Workshop on Operating System Interference in High Performance Applications*, in conjunction with the PACT05 Conference, St. Louis, MO, Sept 2005.
- **M. R. Meswani**, *Improving Throughout of Simultaneous Multithreaded (SMT) Processors using Shareable Resource Signatures and Hardware Thread Priorities,* Ph.D., dissertation, University of Texas at El Paso, College of Engineering – Computer Science, Dec 2009.
- **M. R. Meswani**, *Randomized Protocol for Signing Contracts Digitally*, Masters Project Report, University of Texas at El Paso, College of Engineering – Computer Science, Dec 2000.
- **M. R. Meswani**, et al., *Supply Chain Management for a Computer Store,* B.E Project Report, University of Mumbai, Sardar Patel College of Engineering – Computer Engineering, May 1999.

ACCOMPLISHMENTS AND AWARDS:
- Dodson Ph.D. Completion Fellowship for 2009
- NASA scholarship to attend GRID Summer Workshop 2004
- Awarded Life-time membership in Upsilon Pi Epsilon Honor Society, Dec 2000
- Reliance Undergraduate scholarships for freshman and junior years.